REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 12-11-20	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, OCTAL, 16-BIT DAC WITH 5 ppm/°C ON-CHIP REFERENCE, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12643**
	REV	**PAGE** 1 **OF** 14

AMSC N/A

5962-V027-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance octal, 16-bit DAC with 5 ppm/°C on-chip reference microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12643	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5668-EP	Octal, 16-bit DAC with 5 ppm/°C on-chip reference

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153-AB	Thin Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to GND	-0.3 V to +7.0 V
Digital input voltage to GND	-0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	-0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	-0.3 V to V_{DD} + 0.3 V
Operating temperature range:	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature (T_J max)	150°C
Case outline X:	
Power dissipation	$(T_{J\,MAX} - T_A)/ \theta_{JA}$
θ_{JA} thermal impedance	150.4 °C/W
Reflow soldering peak temperature	
SnPb	240°C
Pb free	260°C

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3 and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Functional block diagram. The functional block diagram shall be as shown in figure 3.

3.5.4 INL – External reference. The INL – External reference shall be as shown in figure 4.

3.5.5 DNL. The DNL shall be as shown in figure 5.

3.5.6 Zero scale error and Offset error vs Temperature. The Zero scale error and Offset error vs Temperature shall be as shown in figure 6.

3.5.7 Gain error and Full scale error vs Supply voltage. The Gain error and Full scale error vs Supply voltage shall be as shown in figure 7.

3.5.8 Digital to Analog glitch impulse (negative). The Digital to Analog glitch impulse (negative) shall be as shown in figure 8.

3.5.9 Serial write operation. The serial write operation shall be as shown in figure 9.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Static performance 3/						
Resolution			16			Bits
Relative accuracy		See FIGURE 4		±8	±21	LSB
Differential nonlinearity		See FIGURE 5 4/			±1	
Zero code error		All 0s loaded to DAC register, See FIGURE 6		1	14	mV
Zero code error drift				±2		µV/°C
Full scale error		All 1s loaded to DAC register, See FIGURE 7		-0.2	-1	% FSR
Gain error					±1	
Gain temperature coefficient		of FSR/°C		±2.5		ppm
Offset error				±1	±14	mV
DC Power supply rejection ratio		V_{DD} ± 10%		-80		dB
DC Crosstalk (External reference)		Due to full scale output change, R_L = 2 kΩ to GND or V_{DD}		10		µV
		Due to load current change		5		µV/mA
		Due to powering down (per channel)		10		µV
DC Crosstalk (Internal reference)		Due to full scale output change, R_L = 2 kΩ to GND or V_{DD}		25		µV
		Due to load current change		10		µV/mA
Output characteristics 5/						
Output voltage range			0		V_{DD}	V
Capacity load stability		R_L = ∞		2		nF
		R_L = 2 kΩ		10		
DC output impedance				0.5		Ω
Short circuit current		V_{DD} = 5 V		30		mA
Power up time		Coming out of power down mode, V_{DD} = 5 V		4		µs
Reference inputs						
Reference current		V_{REF} = V_{DD} = 5.5 V (per DAC channel)		40	55	µA
Reference input range			0		V_{DD}	V
Reference input impedance				14.6		kΩ
Reference outputs						
Output voltage		At ambient	1.247		1.253	V
Reference temperature coefficient 5/				±5		ppm/°C
Reference output impedance				7.5		kΩ
Logic input 5/						
Input current		All digital inputs			±3	µA
Input low voltage	V_{INL}	V_{DD} = 5 V			0.8	V
Input high voltage	V_{INH}	V_{DD} = 5 V	2			
Pin capacitance				3		pF

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
Power requirements						
V_{DD}		All digital inputs at 0 or V_{DD}, DAC active excludes load current	4.5		5.5	V
I_{DD} (normal mode) 6/		$V_{IH} = V_{DD}$ and V_{IL} = GND				
V_{DD} = 4.5 V to 5.5 V		Internal reference off		1.3	1.8	mA
V_{DD} = 4.5 V to 5.5 V		Internal reference on		2	2.6	mA
IDD (All power down modes) 7/						
V_{DD} = 4.5 V to 5.5 V		$V_{IH} = V_{DD}$ and V_{IL} = GND		0.4	1	µA

Test	Symbol	Test conditions 8/	Limits			Unit
			Min	Typ	Max	
AC characteristics						
Output voltage settling time		¼ to ¾ scale settling to ±2 LSB		6	10	µs
Slew rate				1.5		V/µs
Digital to Analog glitch impulse		1 LSB change around major carry , see FIGURE 8		4		nV-sec
Digital feedthrough				0.1		
Reference feedthrough		V_{REF} = 2 V ±0.1 V p-p, frequency = 10 Hz to 20 MHz		-90		dB
Digital crosstalk				0.5		nV-sec
Analog crosstalk				2.5		
DAC to DAC crosstalk				3		
Multiplying bandwidth		V_{REF} = 2 V ±0.2 V p-p		340		kHz
Total harmonic distortion		V_{REF} = 2 V ±0.1 V p-p, frequency = 10 kHz		-80		dB
Output Noise spectral density		DAC code = 0x8400, 1 kHz		120		nV/√Hz
		DAC code = 0x8400, 10 kHz		100		
Output noise		0.1 Hz to 10 Hz		15		µV p-p

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions 9/	Limits			Unit
			Min	Typ	Max	
Timing characteristics						
SCLK cycle time	t_1		20			ns
SCLK high time	t_2		8			
SCLK low time	t_3		8			
$\overline{SYNC}$ to SCLK falling edge setup time	t_4		13			
Data setup time	t_5		4			
Data hold time	t_6		4			
SCLK falling edge to $\overline{SYNC}$ rising edge	t_7		0			
Minimum $\overline{SYNC}$ high time	t_8		15			
$\overline{SYNC}$ rising edge to SCLK fall ignore	t_9		13			
SCLK falling edge to $\overline{SYNC}$ fall ignore	t_{10}		0			
$\overline{LDAC}$ pulse width low	t_{11}		10			
SCLK falling edge to $\overline{LDAC}$ rising edge	t_{12}		15			
$\overline{CLR}$ pulse width low	t_{13}		5			
SCLK falling edge to $\overline{LDAC}$ falling edge	t_{14}		0			
$\overline{CLR}$ pulse activation time	t_{15}			300		

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 1.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range -55°C ≤ T_A ≤ +125°C, Typical at +25°C.

3/ Linearity calculated using a reduced code range of this device (Code 512 to 65,024). Output unloaded.

4/ Guaranteed monotonic by design.

5/ Guaranteed by design, and characterization, not production tested.

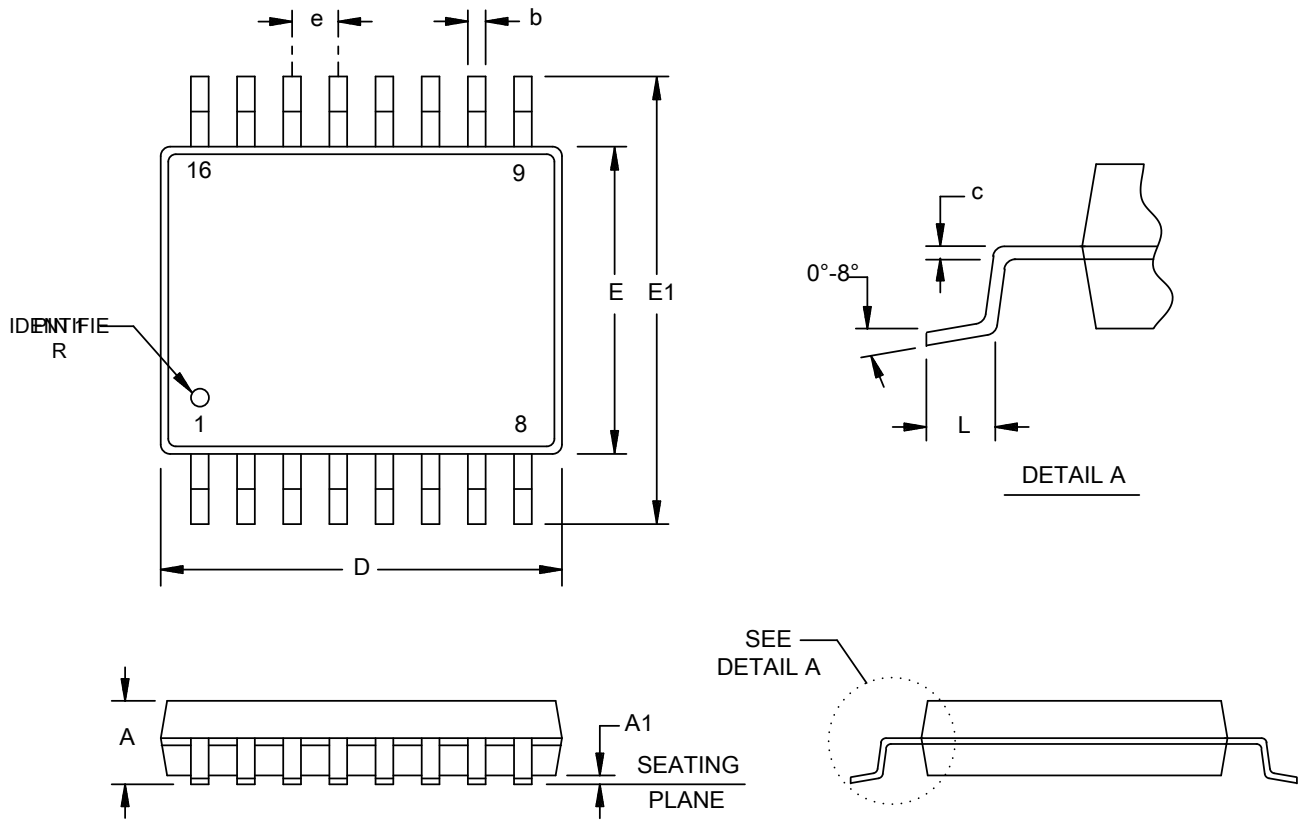
6/ Interface inactive. All DACs active. DAC outputs unloaded.

7/ All eight DACs powered down.

8/ V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Temperature range -55°C ≤ T_A ≤ +125°C, Typical at +25°C.

9/ All inputs signal are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See FIGURE 9. V_{DD} = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 BSC	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-153-AB.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{\text{LDAC}}$	16	SCLK
2	$\overline{\text{SYNC}}$	15	DIN
3	V_{DD}	14	GND
4	$V_{OUT}A$	13	$V_{OUT}B$
5	$V_{OUT}C$	12	$V_{OUT}D$
6	$V_{OUT}E$	11	$V_{OUT}F$
7	$V_{OUT}G$	10	$V_{OUT}H$
8	V_{REFIN}/V_{REFOUT}	9	$\overline{\text{CLR}}$

FIGURE 2. Terminal connections.

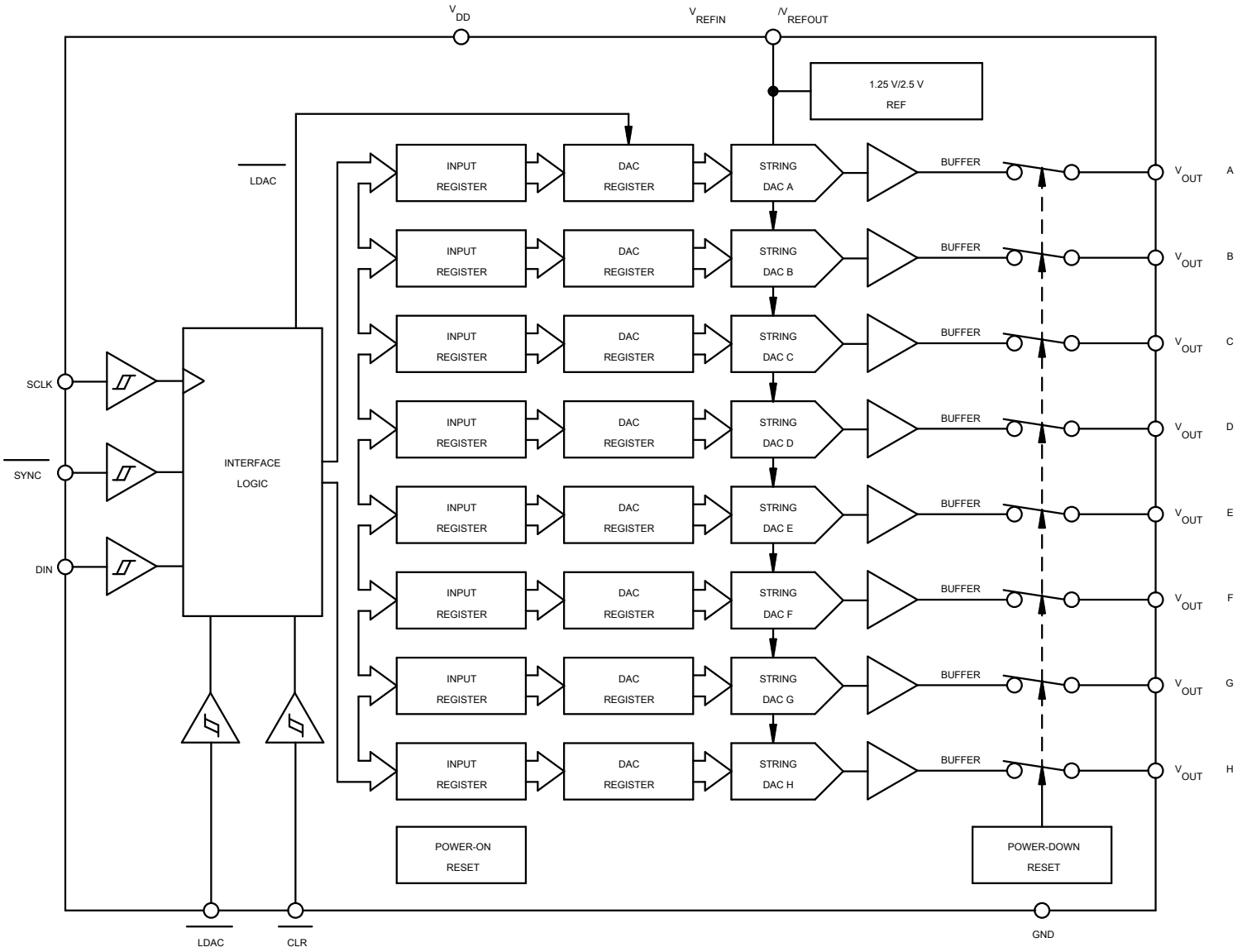


FIGURE 3. Functional block diagram.

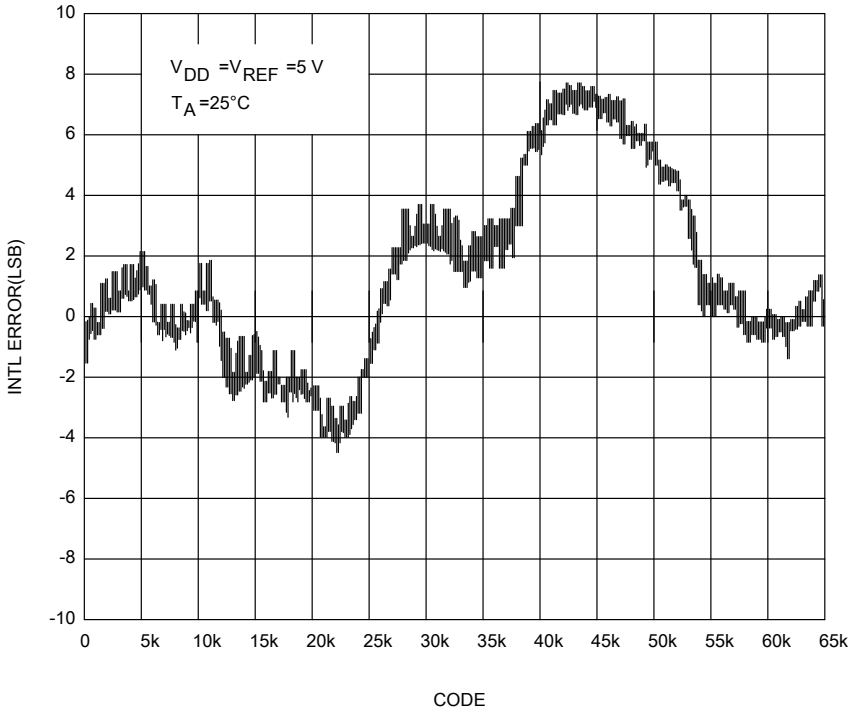


FIGURE 4. INL – External reference.

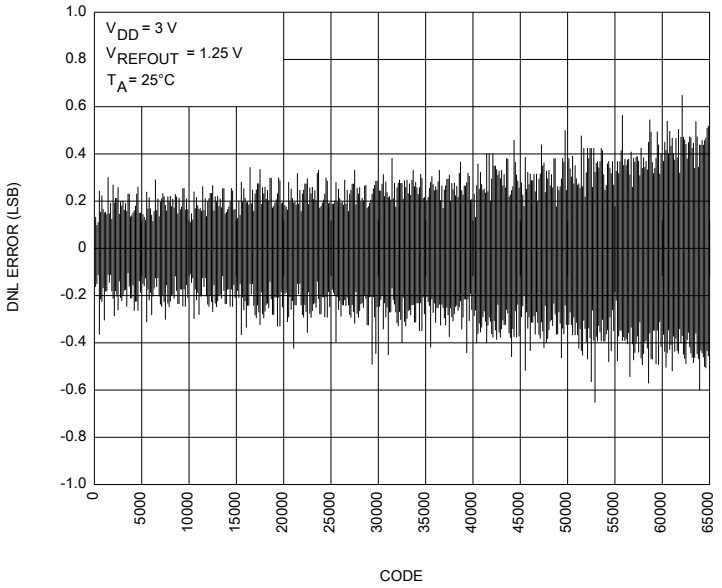


FIGURE 5. DNL.

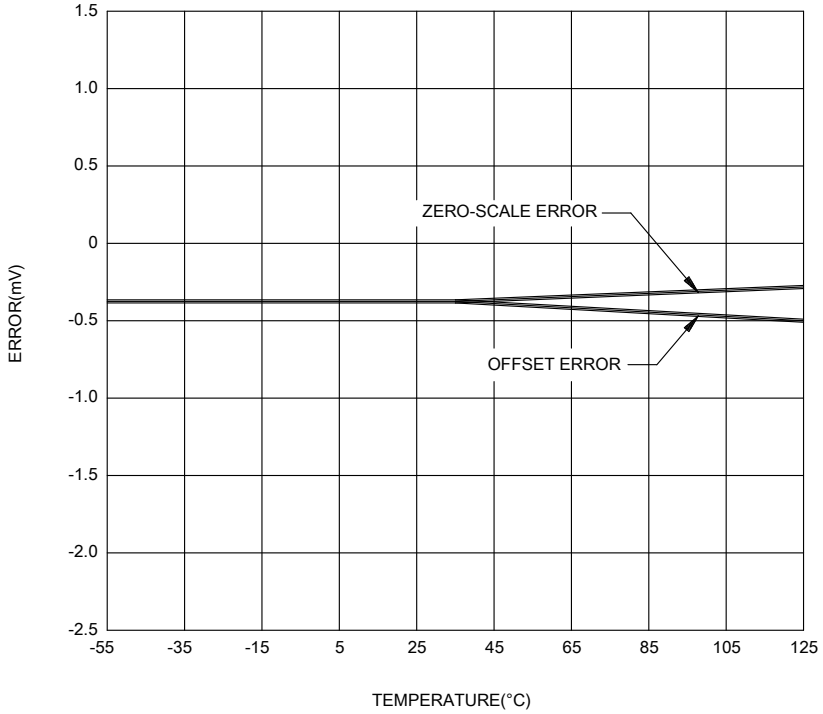


FIGURE 6. Zero scale error and Offset error vs Temperature.

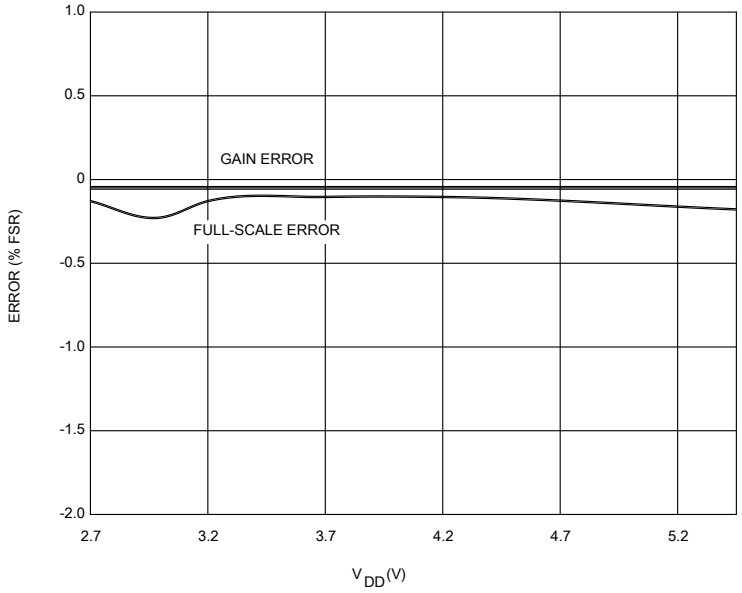


FIGURE 7. Gain error and Full scale error vs Supply voltage.

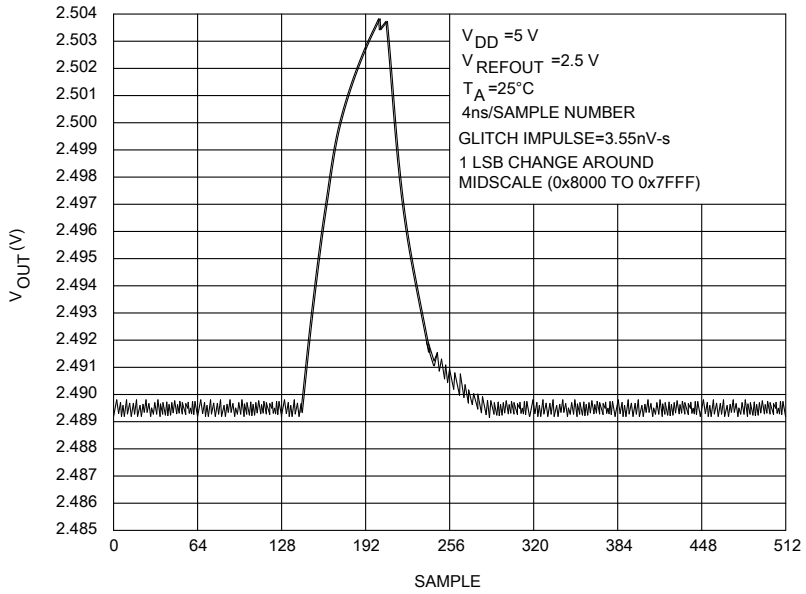
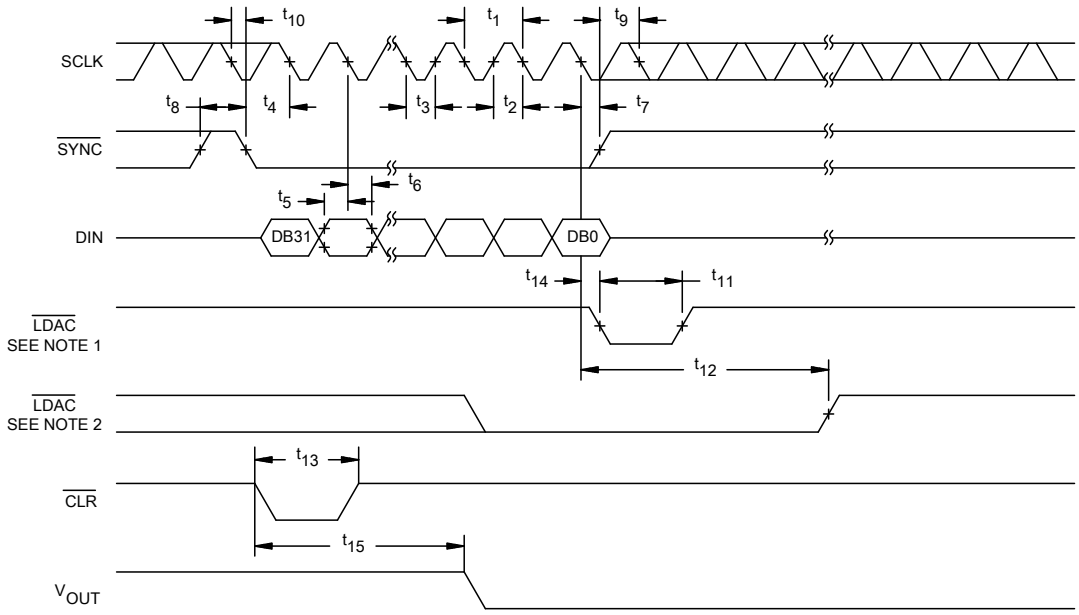


FIGURE 8. Digital to Analog glitch impulse (negative).



NOTES:
1. Asynchronous $\overline{\text{LDAC}}$ update mode.
2. Synchronous $\overline{\text{LDAC}}$ update mode.

FIGURE 9. Serial write operation.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12643-01XB	24355	AD5668SRU-EP-1RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106